Fig. 1

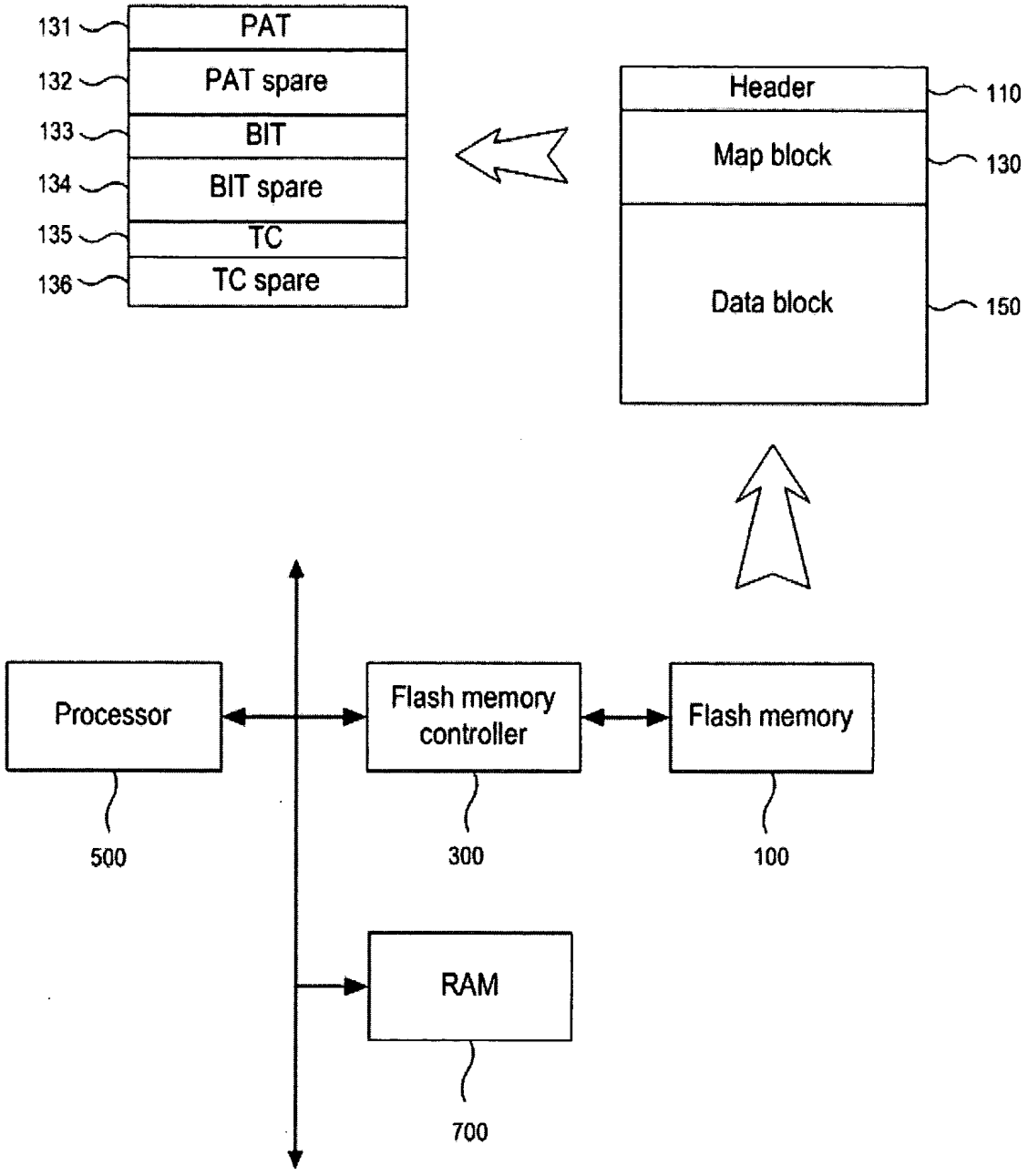
131
PAT
132
PAT spare
133
BIT
134
BIT spare
135
TC
136
TC spare
Header
110
Map block
130
Data block
150
Processor
500
Flash memory controller
300
Flash memory
100
RAM
700

Fig. 2

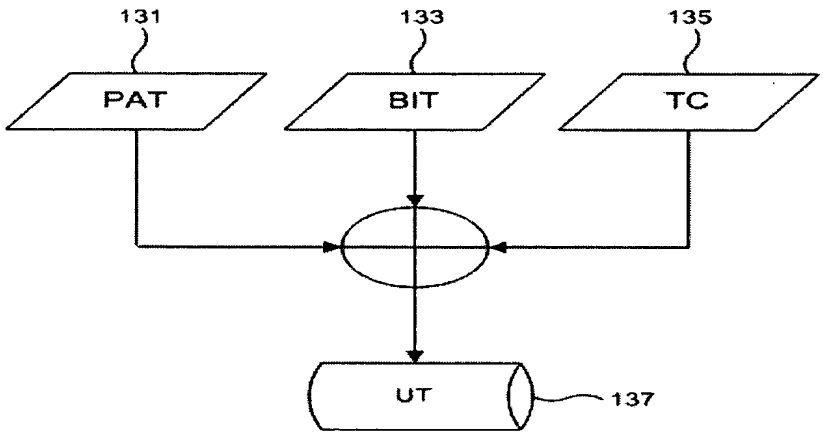

Fig. 3a

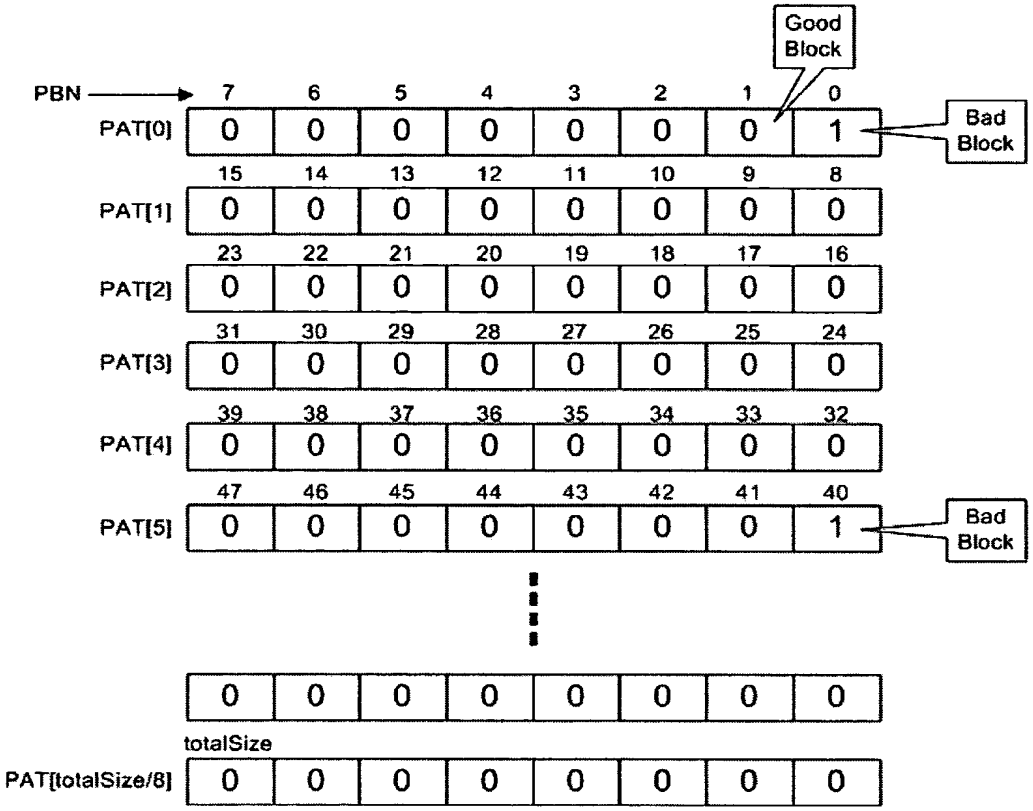
Good Block
PBN
7 6 5 4 3 2 1 0
PAT[0]
0 0 0 0 0 0 0 1
Bad Block
15 14 13 12 11 10 9 8
PAT[1]
0 0 0 0 0 0 0 0
23 22 21 20 19 18 17 16
PAT[2]
0 0 0 0 0 0 0 0
31 30 29 28 27 26 25 24
PAT[3]
0 0 0 0 0 0 0 0
39 38 37 36 35 34 33 32
PAT[4]
0 0 0 0 0 0 0 0
47 46 45 44 43 42 41 40
PAT[5]
0 0 0 0 0 0 0 1
Bad Block
0 0 0 0 0 0 0 0
totalSize
PAT[totalSize/8]
0 0 0 0 0 0 0 0

Fig.3b

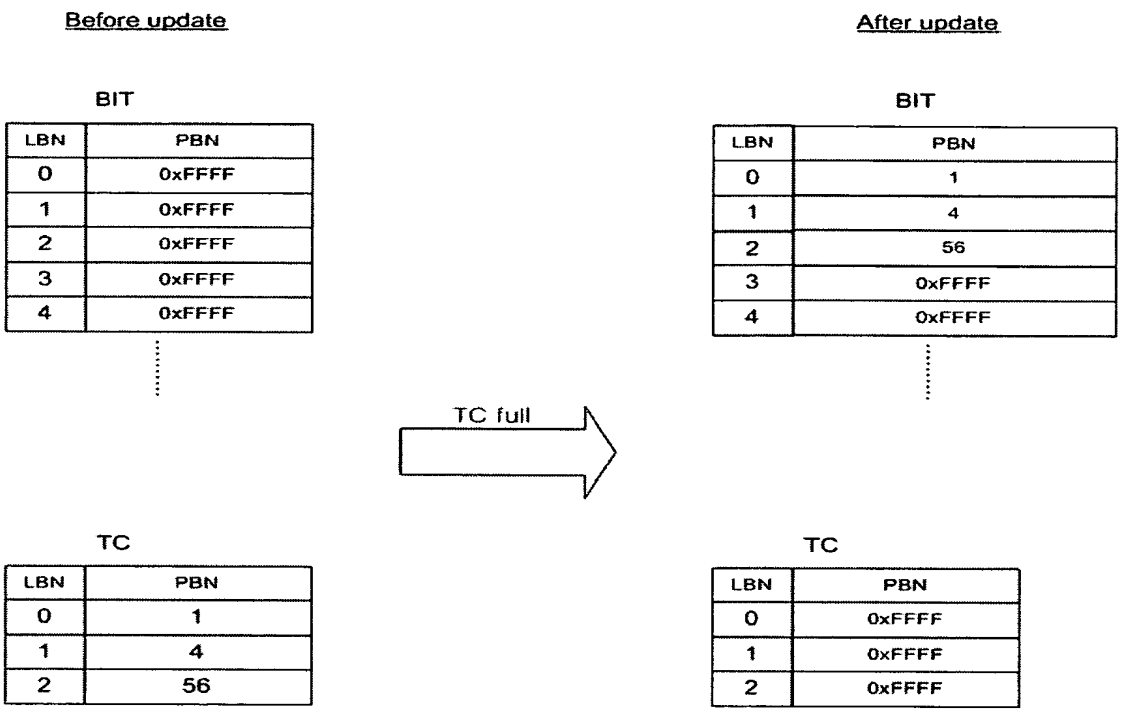
Before update
After update
BIT
LBN
PBN
0
0xFFFF
1
0xFFFF
2
0xFFFF
3
0xFFFF
4
0xFFFF
BIT
LBN
PBN
0
1
1
4
2
56
3
0xFFFF
4
0xFFFF
TC full
TC
LBN
PBN
0
1
1
4
2
56
TC
LBN
PBN
0
0xFFFF
1
0xFFFF
2
0xFFFF

Fig. 3c

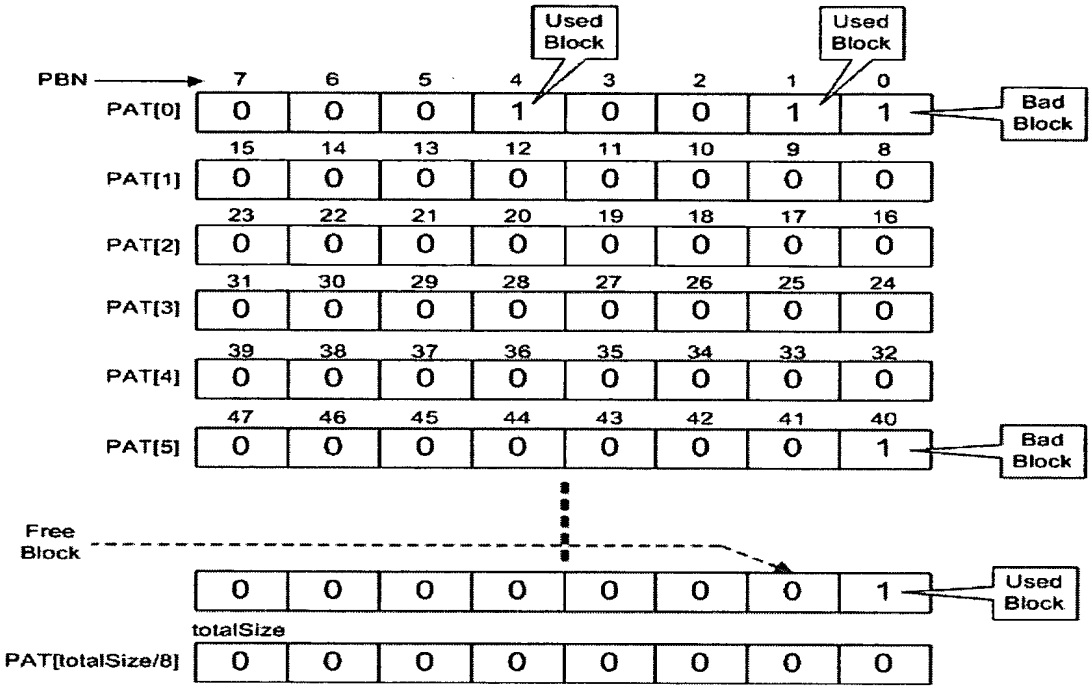
Used Block
Used Block
PBN
7 6 5 4 3 2 1 0
PAT[0]
0 0 0 1 0 0 1 1
Bad Block
15 14 13 12 11 10 9 8
PAT[1]
0 0 0 0 0 0 0 0
23 22 21 20 19 18 17 16
PAT[2]
0 0 0 0 0 0 0 0
31 30 29 28 27 26 25 24
PAT[3]
0 0 0 0 0 0 0 0
39 38 37 36 35 34 33 32
PAT[4]
0 0 0 0 0 0 0 0
47 46 45 44 43 42 41 40
PAT[5]
0 0 0 0 0 0 0 1
Bad Block
Free Block
0 0 0 0 0 0 0 1
Used Block
totalSize
PAT[totalSize/8]
0 0 0 0 0 0 0 0

Fig. 4

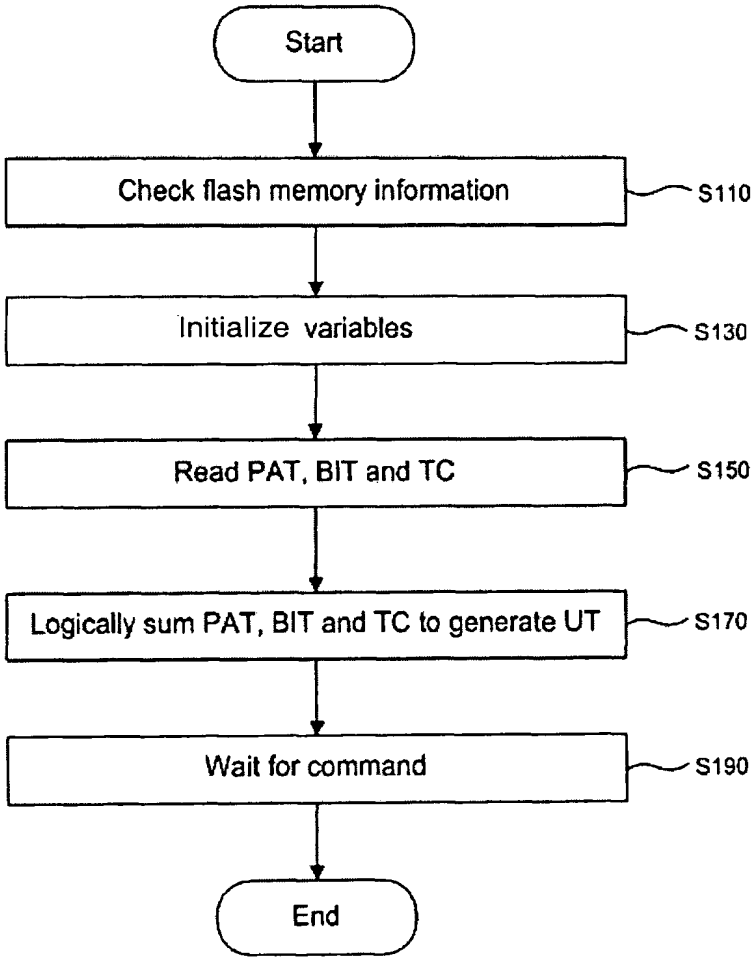
Start
Check flash memory information
S110
Initialize variables
S130
Read PAT, BIT and TC
S150
Logically sum PAT, BIT and TC to generate UT
S170
Wait for command
S190
End

Fig. 5

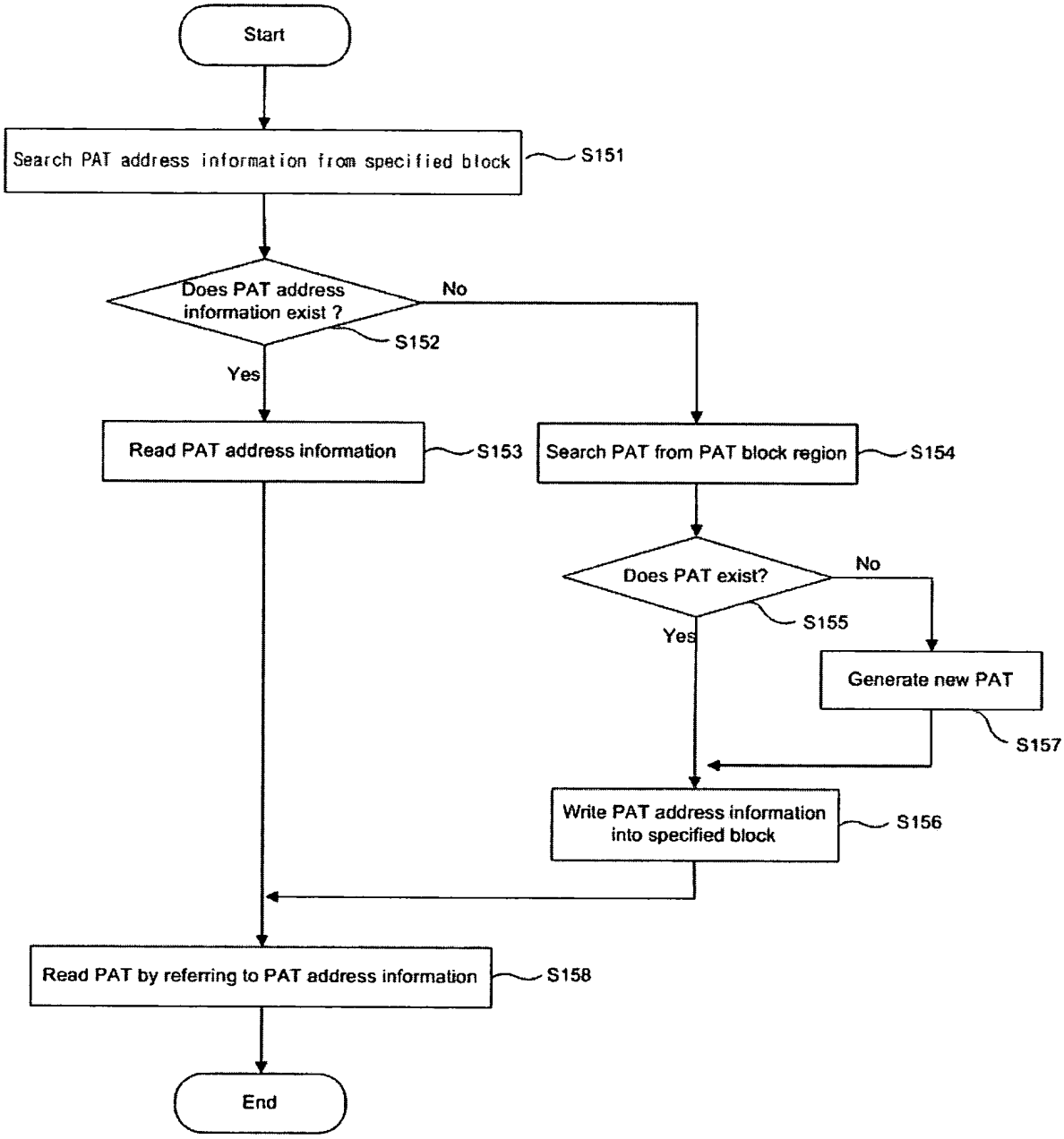
Start
Search PAT address information from specified block
S151
Does PAT address information exist ?
No
S152
Yes
Read PAT address information
S153
Search PAT from PAT block region
S154
Does PAT exist?
No
S155
Yes
Generate new PAT
S157
Write PAT address information into specified block
S156
Read PAT by referring to PAT address information
S158
End

Fig. 6

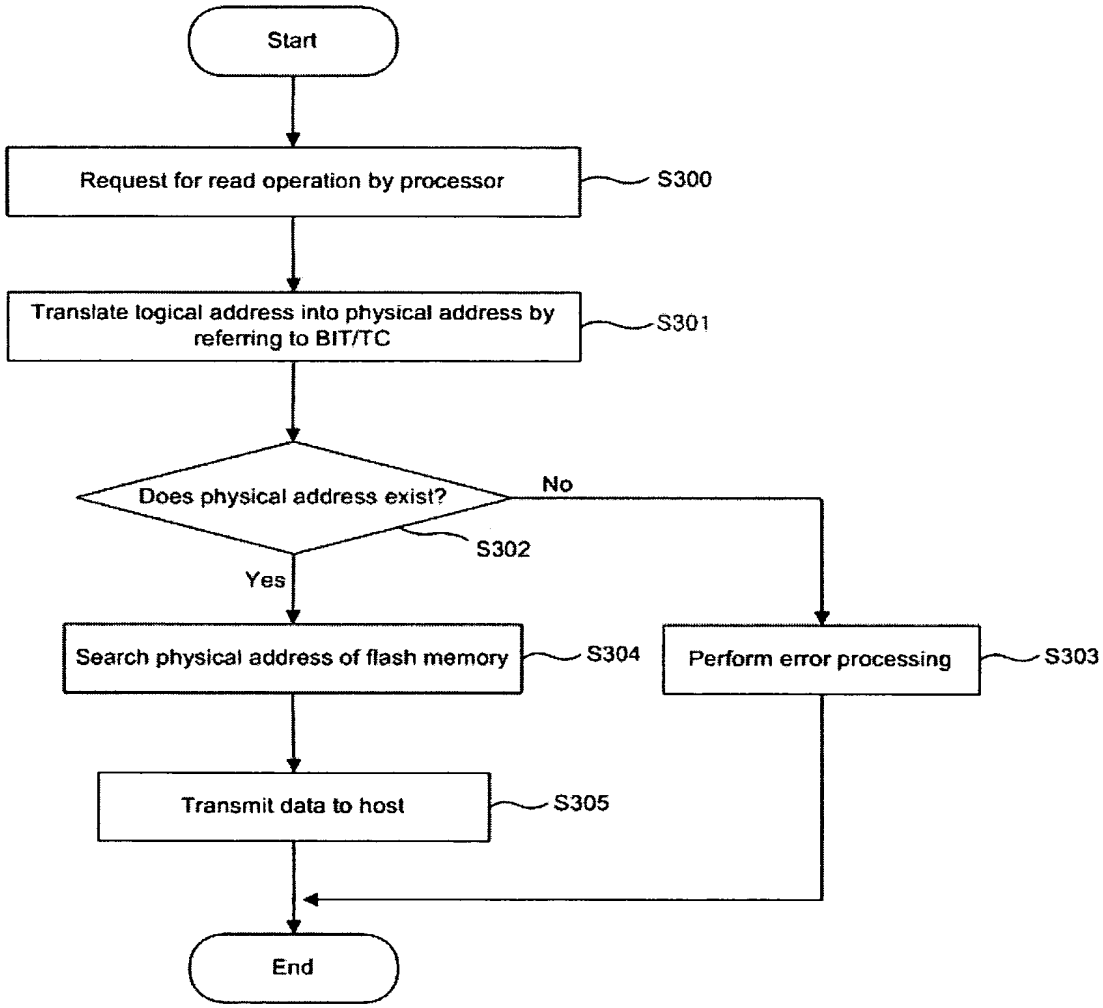
Start
Request for read operation by processor
S300
Translate logical address into physical address by referring to BIT/TC
S301
Does physical address exist?
No
S302
Yes
Search physical address of flash memory
S304
Perform error processing
S303
Transmit data to host
S305
End

Fig. 7

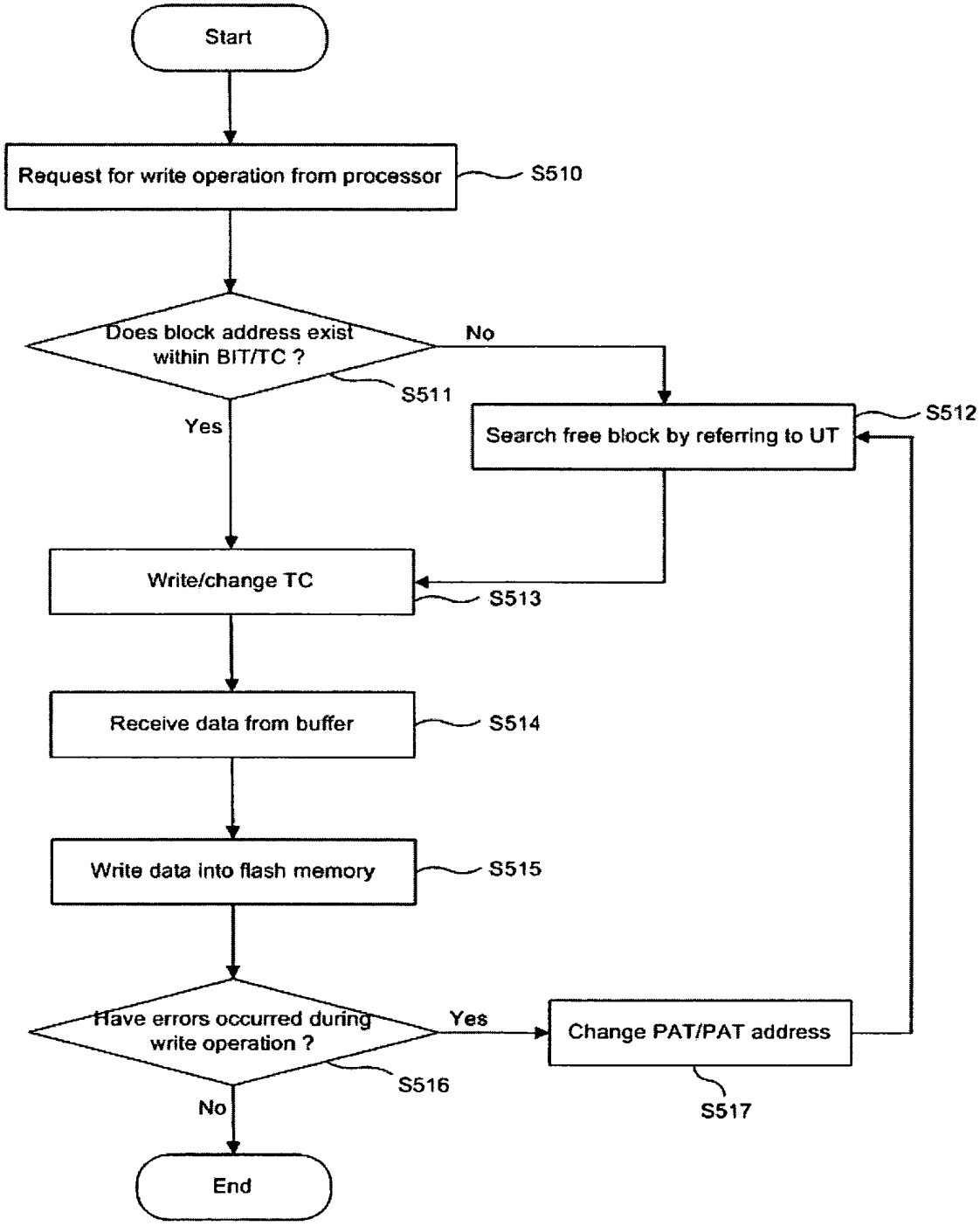
Start
Request for write operation from processor
S510
Does block address exist within BIT/TC ?
No
S511
Yes
Search free block by referring to UT
S512
Write/change TC
S513
Receive data from buffer
S514
Write data into flash memory
S515
Have errors occurred during write operation ?
Yes
S516
Change PAT/PAT address
S517
No
End

Fig. 8

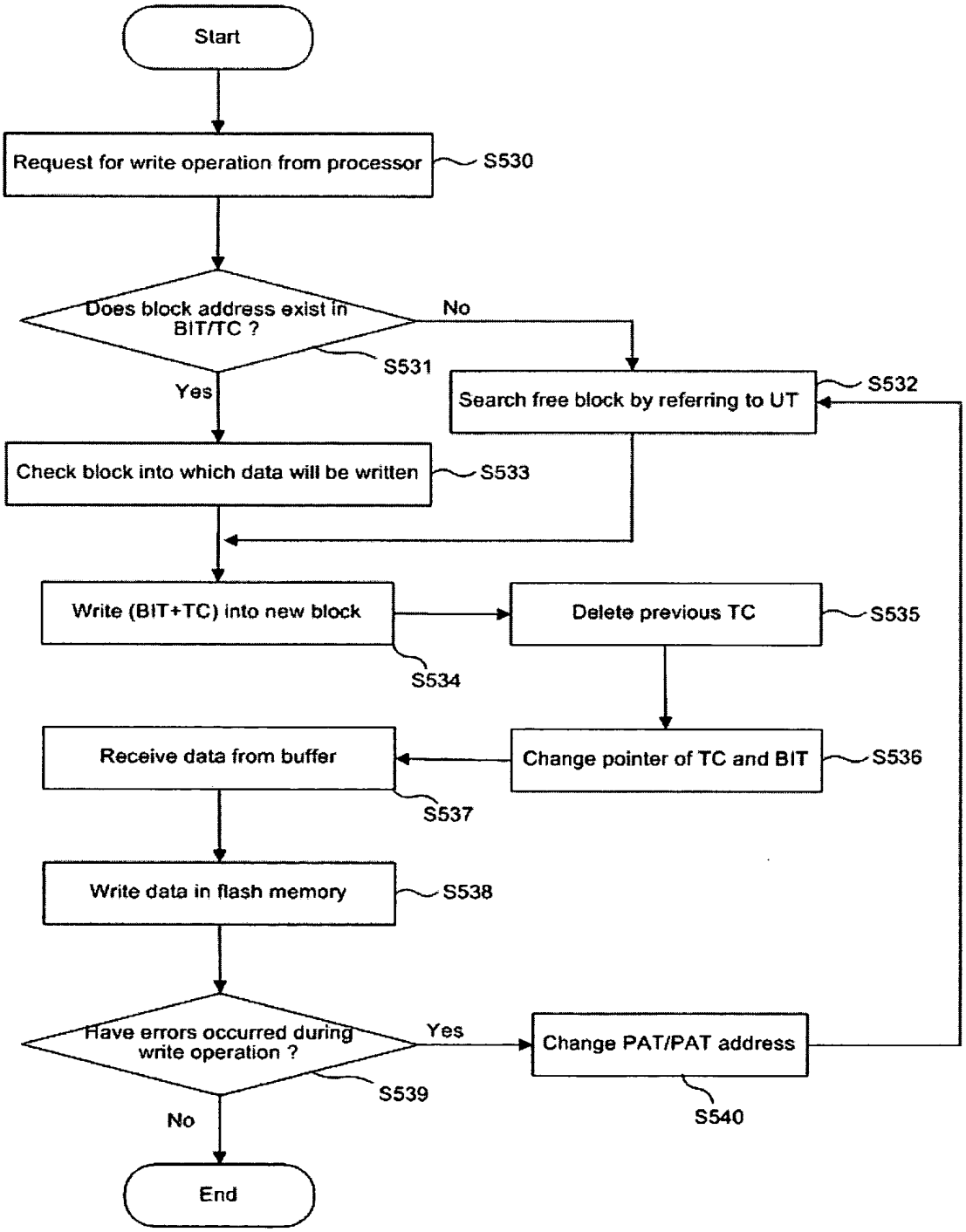
Start
Request for write operation from processor
S530
Does block address exist in BIT/TC ?
S531
No
Yes
Search free block by referring to UT
S532
Check block into which data will be written
S533
Write (BIT+TC) into new block
S534
Delete previous TC
S535
Change pointer of TC and BIT
S536
Receive data from buffer
S537
Write data in flash memory
S538
Have errors occurred during write operation ?
S539
Yes
No
Change PAT/PAT address
S540
End

Fig. 9

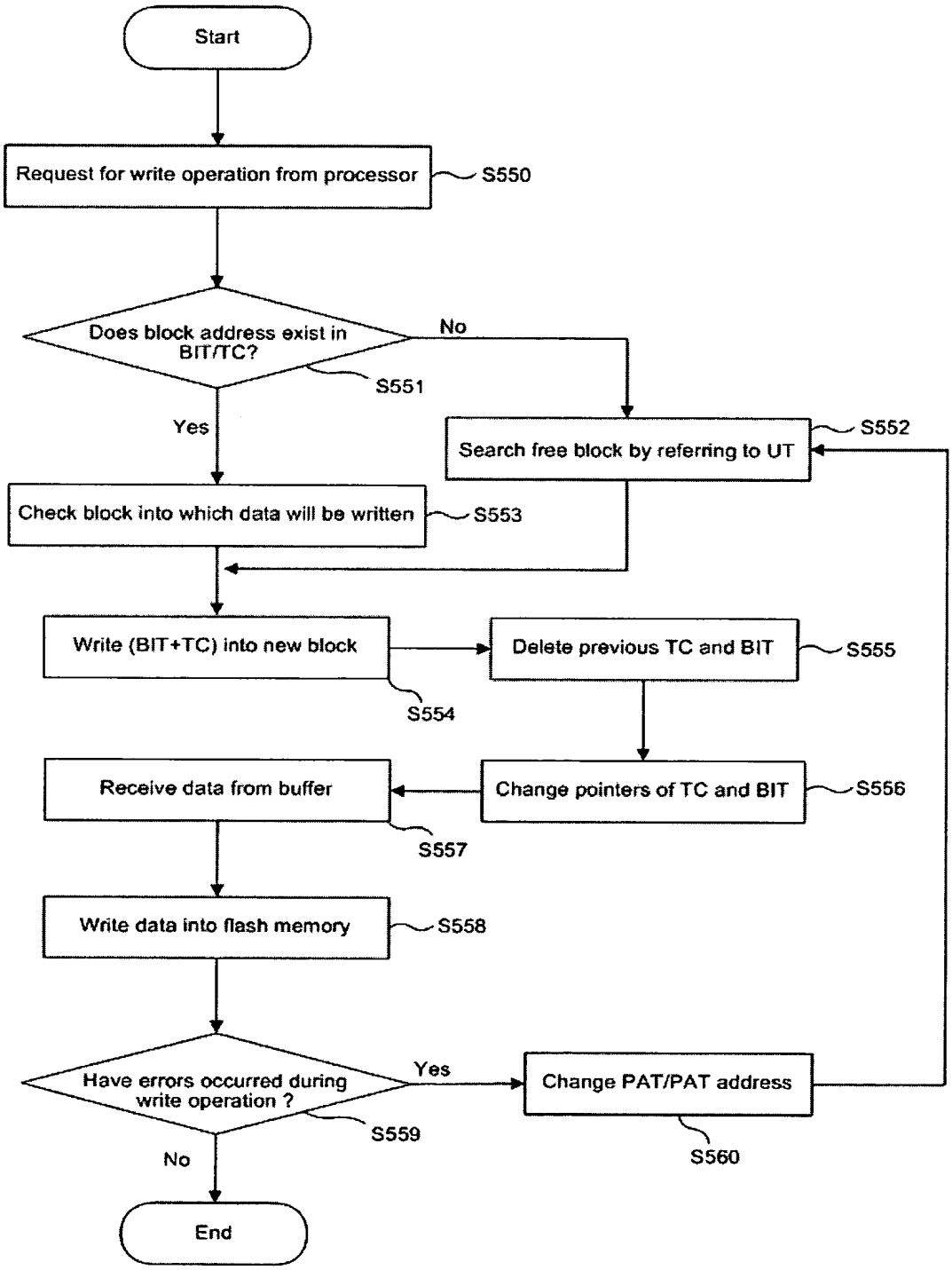
Start
Request for write operation from processor
S550
Does block address exist in BIT/TC?
S551
No
Yes
Search free block by referring to UT
S552
Check block into which data will be written
S553
Write (BIT+TC) into new block
S554
Delete previous TC and BIT
S555
Change pointers of TC and BIT
S556
Receive data from buffer
S557
Write data into flash memory
S558
Have errors occurred during write operation ?
S559
Yes
No
Change PAT/PAT address
S560
End

Fig. 10

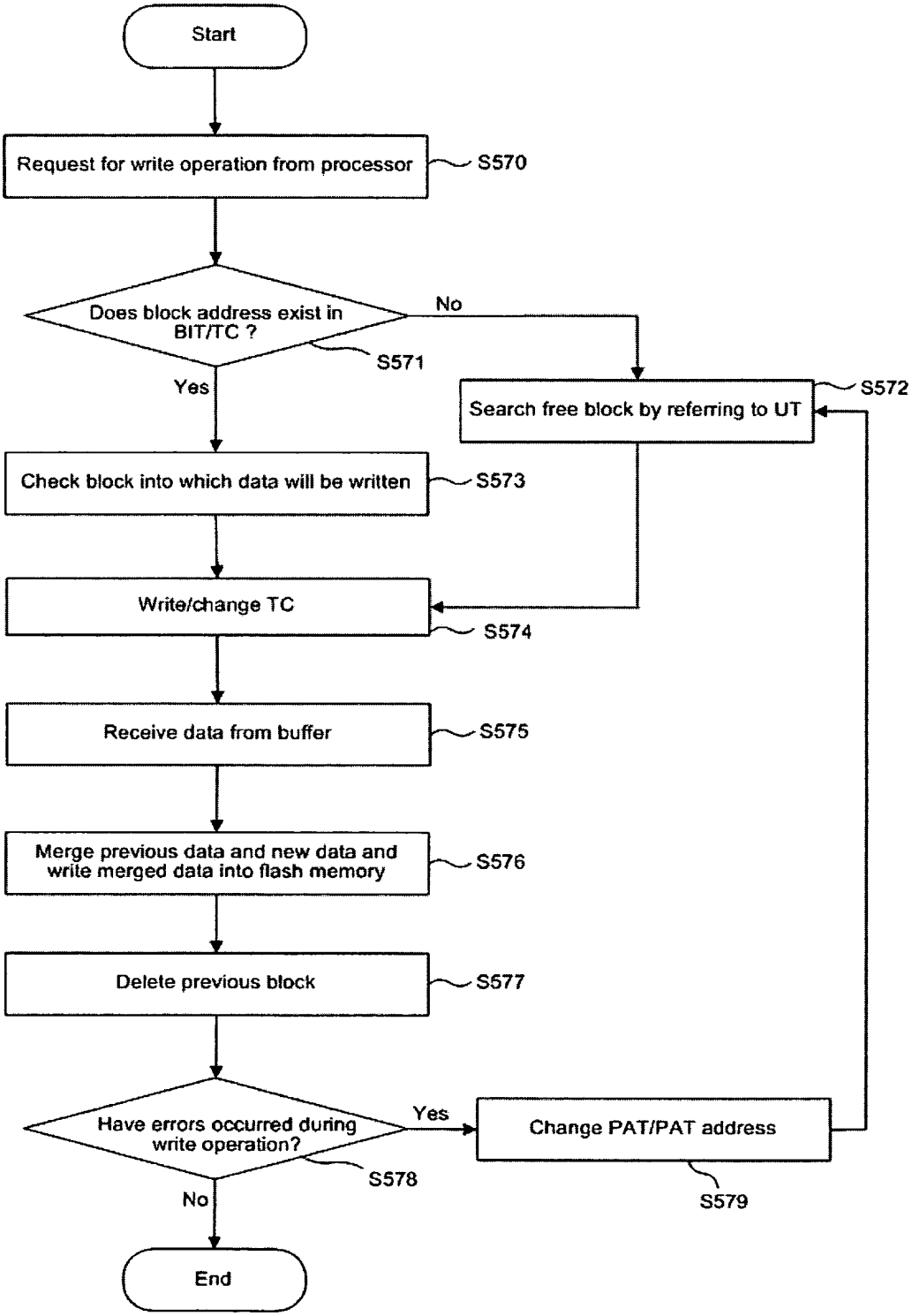
Start
Request for write operation from processor
S570
Does block address exist in BIT/TC ?
S571
No
Yes
Search free block by referring to UT
S572
Check block into which data will be written
S573
Write/change TC
S574
Receive data from buffer
S575
Merge previous data and new data and write merged data into flash memory
S576
Delete previous block
S577
Have errors occurred during write operation?
S578
Yes
No
Change PAT/PAT address
S579
End

Fig. 11

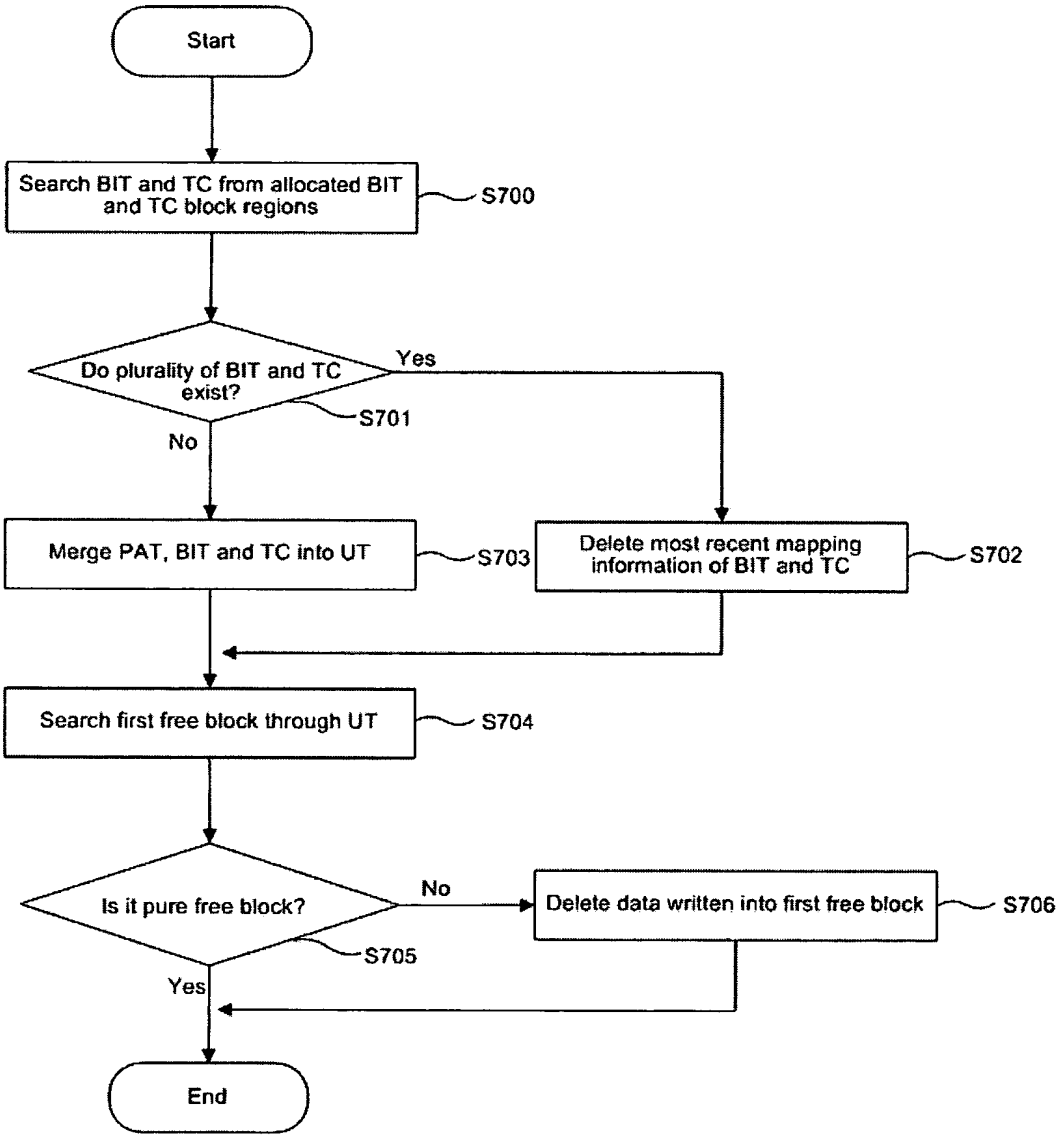
Start
Search BIT and TC from allocated BIT and TC block regions
S700
Do plurality of BIT and TC exist?
Yes
S701
No
Merge PAT, BIT and TC into UT
S703
Delete most recent mapping information of BIT and TC
S702
Search first free block through UT
S704
Is it pure free block?
No
S705
Delete data written into first free block
S706
Yes
End

Fig. 12a

TC

LBN	PBN
0	1
1	4
2	0xFFFF

BIT

LBN	PBN
0	0xFFFF
1	0xFFFF
2	0xFFFF

Fig. 12b

TC

LBN	PBN
0	1
1	4
2	56

LBN(1)=PBN(4)

Power cutoff

BIT

LBN	PBN
0	1
1	0xFFFF
2	0xFFFF

TC spare

LBN	PBN
0	1
1	4
2	56

Fig. 12c

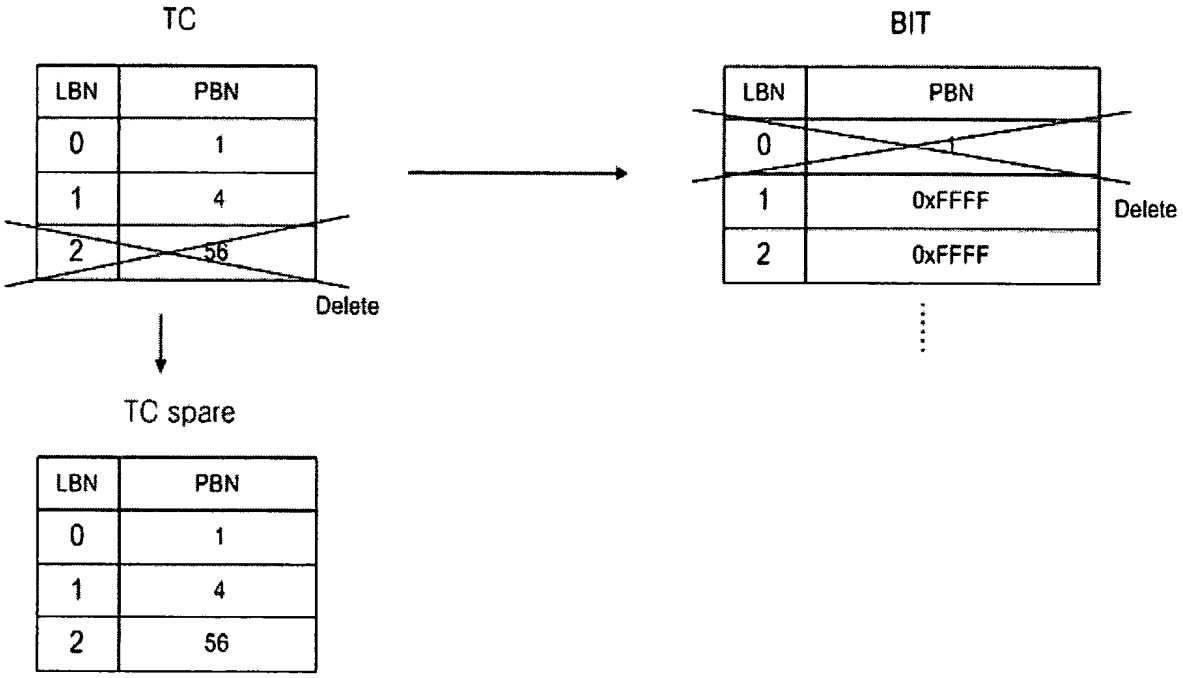
TC
LBN
PBN
0
1
1
4
2
56
Delete
TC spare
LBN
PBN
0
1
1
4
2
56
BIT
LBN
PBN
0
1
1
0xFFFF
2
0xFFFF
Delete

Fig. 13a

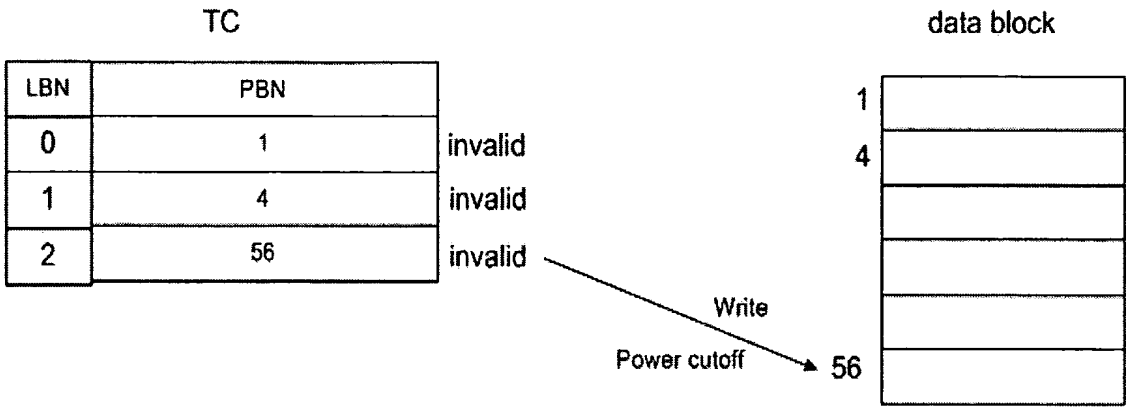

Fig. 13b